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A MICROSWITCH BASED P.I.N DIODE SWITCH

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ABSTRACT

The behaviour of semiconductor devices at the microwave frequencies could be easily understood when the devices are represented by lumped networks. This paper has shown that the diode because of its smallness compared to the wavelength of the applied field could be used as a lumped element and the p-i-n diode serves as a good candidate for this purpose. The forward and reverse were seen to follow near normal diode characteristics bias impedences. The effect of insertion loss or minimum attenuation as well as impact of isolation on attenuation were verified. These effects were tested on P-I.N diode for single and multiple throw switches. The work showed that for two single switching circuits, there was minimum transmission coefficient of 0.94 at 3.2GHz and maximum of 0.11 at zero bias. For double switching grant, the minimum transmission coefficient was 0.92 with a maximum of 0.07. The isolation increase as the number of diodes increased, moving from 44db for double diode circuit to 53.9dB for three.

Key Words: *Lumped elements, transmission coefficient, insertion loss, isolation, attenuation, reactive element matching.*

INTRODUCTION

The use of a semiconductor device in any application requires an accurate knowledge of the behaviour of the device. At microwave frequencies, the behaviour of semiconductor devices is most readily predicted if the devices are represented by lumped element networks. However, it must be said that at the higher end of the microwave region, the use of such lumped element representation is limited in accuracy. This is because at these frequencies, the physical components of the device exhibit distributed characteristics.

Below 15GHz, the use of these lumped elements can be very good for circuits confined to electrically small regions. Since a diode is ordinarily small compared to the wavelength of the applied field, lumped element representation can be used. The exact nature of the lumped elements representing a p.i.n diode circuit is derived. Though there have been some works on the derivation of p.i.n diode equivalent circuit, most of these works have given rise to complex networks which are to difficult to incorporate in an analysis program (Chaffin 1973, Nason 1909). For most analysis, a simplified equivalent circuit can be constructed without serious loss of accuracy.

The equivalent circuit used here was derived by considering the diode behavior in each bias stage and taking into account only those diode parasitic elements which are significant in each bias state.

Basic Theory

The p.i.n diode consists of a semiconductor wafer which is mounted on a package as shown in fig.1 Each of the flat surfaces is heavily doped with boron and phosphorous to form the p- and n- layers respectively. These are separated by a weekly doped layer of high resistivity intrinsic material. Electrical contacts are made to the two heavily doped layers. The doping profile of the device is shown in fig 2. In practice, a true intrinsic layer does not exist in a p-i-n diode. This is because it has not been technologically feasible to maintain intrinsic resistivity in the layer through the processing of a diode. In effect, the lightly doped high resistivity region is a p-i or n layer depending on whether the conductivity is a p-n or n – respectively. The difference between an ideal p.i.n diode which has an intrinsic layer and a practical diode in which the layer is actually a p-i can be compared by considering what happens to the

space charge density and the electric field distribution of both as reverse bias is applied to them.

At zero bias, the diffusion of holes and electrons across the junction causes space charge regions to form the p- and n- layers adjacent to the intrinsic layer. For the ideal diode, which has an intrinsic layer that has no impurities, the layer is completely depleted of mobile carriers. Thus we have a region of fixed negative charge in the p-layer and a region of fixed positive charge in the n-layer with no charge in the i-layer as shown in fig 2(a). As reverse bias is applied to the diode, a uniform electric field appears in the i-layer and this drops linearly to zero through the depletion regions in the p- and n-layer, as illustrated in fig 2(b).

If the high resistivity region is a p-i layer, then with no applied bias, the diffusion of holes and electrons across the n-pi junction will produce a very thin depletion region in the n-layer and a thicker depletion region in the pi layer. As reverse bias is applied, the depletion region becomes thicker until the entire pi layer is swept free of mobile carriers. Increasing this bias does not produce significant changes in the regions. The conclusion drawn from the above comparison is that the intrinsic layer of an ideal diode is completely swept at zero or any reverse bias whereas in a practical diode, a small bias must be used to sweep out the intrinsic or i-layer. This means that measurements made under zero bias condition does not accurately represent the reverse bias behavior of the diode.

As a reverse bias voltage is applied to the diode a large current begins to flow immediately, this current being limited only by the impedance of the voltage source. The intrinsic region will be completely depleted of mobile carriers. When this happens, the conductivity of the diode decreases and the total impedance of the diode becomes essentially a constant capacitance in series with a very high resistance. This condition is represented by the capacitance C_d and the reverse resistance R_r in fig 3. This capacitance is independent of the applied bias. This is because any further increase in the applied voltage does not increase the thickness of the depletion region.

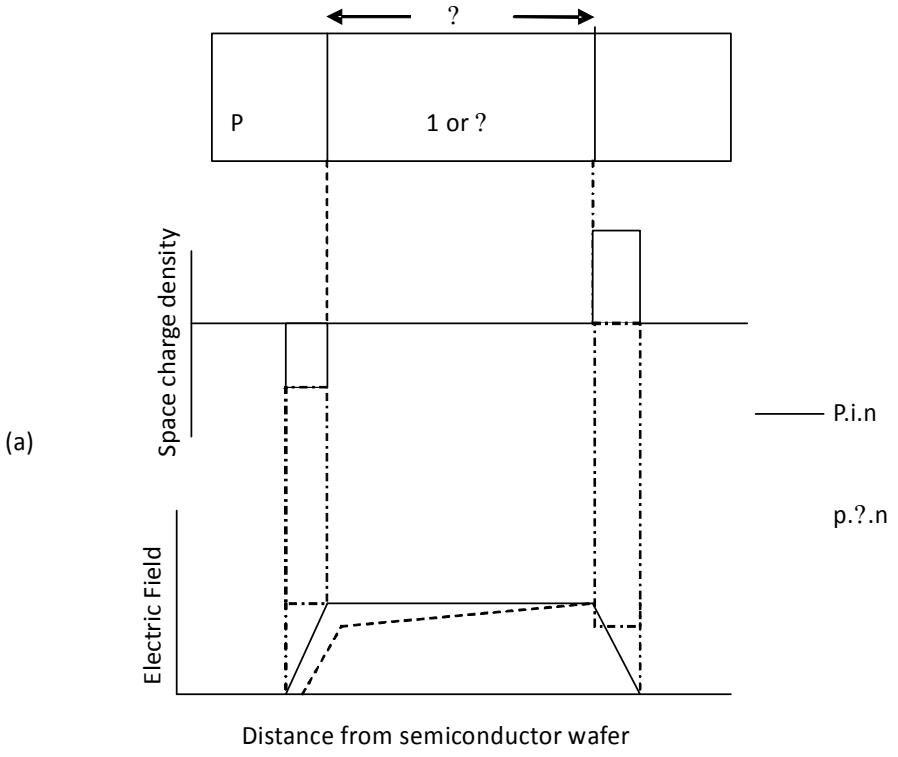

Fig. 1: Charge and field distribution in p.i.n and p.?.ν φυνχτιον

When forward bias is applied to the diode, the intrinsic layer becomes flooded with injected carriers. Electrons are injected into the region from the n-layer and holes from the p-layer. As the carriers diffuse into this intrinsic region their concentration diminishes with the depth of the region. When this happens, the diode exhibits very low resistance and appears as a virtual short circuit across the transmission line. This condition is represented by the forward resistance R_f and the series inductance L_s in fig 3. Unlike the reverse bias capacitance, the value of the forward resistance is a function of the applied bias. A certain amount of bias is required before the lowest value of forward resistance can be attained.

The diode is usually mounted on a package so that it may be conveniently handled. This package contributes its own parasitic reactances represented by L_p and C_p. The values of these components can easily be determined as will be shown later

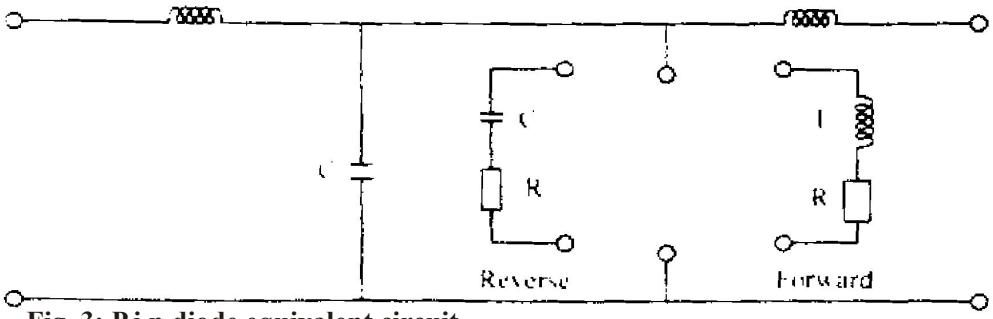

Fig. 3: P.i.n diode equivalent circuit

the equivalent circuit elements of the diode can be determined by measuring the loss produced by the diode and then deducing the values of the elements using graphical techniques. When the diode is forward biased, the resulting loss is given by (Hapgood, 1981).

$$= 20\log [\, 1 + Z_0/2Z_d]\text{dB}$$

Where Z_d is the diode impedance and Z_0 is the characteristic impendence of the line. From the fig 3 the diode impedance under forward bias is given by

$$Z_j = \frac{R_1}{(1-W^k\ L_{p\,C_p})2+(W\ C_{p\,R_1})} + j\ \ wL$$

$$+\ \frac{wLp(1-W^k\ L_{p\,C_p})-W\ L_{p\,R^2{}_1}}{(1-W^2\ L_{p\,C_p})2+(W\ C_{p\,R_1})} \quad (2)$$

To simplify matters, it was assumed that

$$(1 - W^2\ L_{p\,C_p})\,2$$

$$C_pR^2{}_j << L_p\,(1 - w^2\ L_pC_p) << 1$$

$$\text{Hence } Z_j = R_1 + jwL_n$$

(3)

Where $L_n = (L_p + {}_S)$

Thus $x = 20\log[1+Z/2(R_1 + jwL_a)'\text{dB}$ (4)

This was re-arranged in the form

$$1/(A-1) = (w^2L_n + R^2{}_1)/(R_1 + Z_0/4)Z_0$$

(5)

Where $A = 10^{v10}$

Equation (5) is in the form of y = mx + C

EXPERIMENTATION AND ANALYSIS

3.1 p-i-n Diode

By measuring the diode impedance forward bias and then using these values, a graph of 1/(A-1) against w^2 can be plotted as shown in fig 4. By process of extrapolation, the values of L_n and R_f can be obtained from the gradient and intercept respectively.

Knowing L_n, the values of the package inductance L_p can be found by relating the geometry of the diode leads to that of the microstrip line. Although this is an approximation, it is the only known method of evaluating this element. The dimensions of the

package leads are given in fig. 3. Basic transmission line theory gives this inductance as;

$$L_p = {}^{Z}{}_{p} \sin {}^{(2\pi e/\lambda g/w)}/_{w}$$

(32)

Where e is the length of the diode and Z_p is the equivalent impedance of the line. These measurements are usually made at the lower microwave range where the effects of the package capacitances C are neglected. At frequencies above 2GHz, these elements become significant. To find C_p the frequency of minimum isolation is noted. This frequency corresponds to a parallel resonance of L_n and C_p. Since the value of L_n is already known, C_p can be obtained from the relation.

$$Cp = 1/w^2\ Lp$$

(33)

The principles used above can equally be adopted to find the reverse bias elements. When the diode is reverse biased, the impedance from fig 9.3 becomes

$$Z_j = \frac{R_1}{(1-w^k\ L_{p\,C_p})2+(W\ C_{p\,R_1})} + j\quad wL$$

$$+\frac{wLp(1-w^k\ L_{p\,C_p})-W\ L_{p\,R^2{}_1}}{(1-w^2\ L_{p\,C_p})2+(W\ C_{p\,R_1})}$$

Using similar assumptions as before, this reduces to

$Z_r\ R_r + jX_r$

Where $X_r = wC(wL_n - 1/wC_d)$

(34)

Fig 5 shows the graph under reverse bias. Here the frequency of maximum insertion loss corresponds to a series resonance of L_n and C_d. Since the value of L_n is already known, the value of C_d can easily be obtained from the relation.
$C_d = 1/w^2L_n$

(35)

The measurement also yields the value of R_r because the attenuation at this frequency is given by

$$x = 20\log[1+Z_0/2R_r]$$

(36)

since this attenuation is known, R_r can be evaluated.

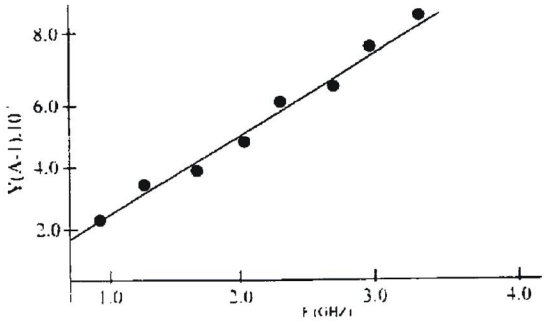

Fig. 4: Forward Bias condition

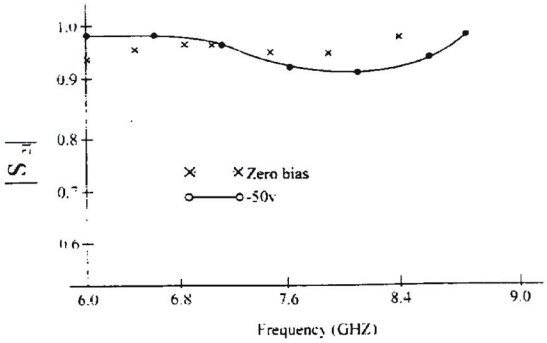

Fig. 5: Reverse bias condition

2.2 Single Pole Single Throw Switch

The RF power incident on an ideal attenuating device is either absorbed or transmitted past the device with no power reflected. The attenuation of the device is defined as the ratio in decibels of the incident power to the reflected power. If the attenuation of the device can be changed from some low value to some high value the device is called a switch. The insertion loss is defined as the minimum attenuation and the isolation is defined as the maximum attenuation. When a diode is inserted in series or in shunt in a transmission line, the radio frequency power incident on the diode is reflected by, absorbed in

or transmitted past the diode. A diode is different from an attenuating device in that most of the incident radio frequency power not transmitted is reflected rather than absorbed. In fact, in an ideal diode switch, the incident power is either completely reflected or completely transmitted. The definition of attenuation, insertion loss and isolation are the same for a diode switch as for an absorption switch.

The radio frequency power transmitted past the diode is in all cases the power delivered to the matched load. The incident RF power must be visualized as the forward travelling wave incident on the diode. For the purpose of deriving the attenuation resulting from impedance and admittance, the diode is visualized as a two terminal device whose RF impedance can be varied by changing the applied voltage. Let V be the peak amplitude of the sinusoidal voltage source which is assumed to have an output impedance Z_0, Z represents that of the diode, I is the peak amplitude of the resulting sinusoidal current. The power in the load is given by

$$P_L = 0.5II^*Z_0 \quad (6)$$

If $Z = R + jX$, then the power P_1 transmitted to the load is given by

$$P_1 = \frac{V^2 Z_0}{2(R+2Z_0)^2 + X^2} \quad (7)$$

The power P_1 incident on the diode is the power in the forward travelling wave going towards the load. This is attained in the series connected diode by setting Z equal to zero. Hence

$$P_1 = V^2/8Z_0 \quad (8)$$

and the resulting attenuation is given by (9)

$$x = 10\log P_1/P_1$$
$$= 10\log \frac{(R/Z_0 + 2)^2 + (X/Z_0)^2}{4} \quad (10)$$

For a diode in shunt having an admittance $Y = G + jB$, the derivation of attenuation is the same as above with the substitution of Y for Z. I for V. etc thus.

$$P_L = 0.5V.\ V^*Y_0 \quad (11)$$

$$\text{And } x = 10\log \frac{(G\,Y_0 + 2)^2 + (B\,Y_0)^2}{4} \quad (12)$$

Where higher isolation is required than is possible with one diode, two or more diodes may be used. The total isolation from multiple diodes is a function of the spacing between them. At optimum spacing, the total isolation is greater than the sum of individual isolations. For the theoretical analysis, the diodes in the isolation state are considered to be equal, lossless reactance. The spacing between two equal reactances for minimum reflected power is a function of their normalize reactance. For maximum reflected power, the spacing $L/_g$ is a quarter wavelength different from that for minimum reflection as shown below. One shunt susceptance element with a match load behind it results in a normalized admittance of

$$Y/Y_0 = 1 + jB/Y_0 \quad (13)$$

This can be matched out or compensated by placing a second equal shunt susceptances a distance e towards the generator which render the first admittance.

$$Y/Y_0 = 1 + jB/Y_0 \quad (14)$$

$$= \frac{\lambda}{2\pi} \tan^{-1} \left[\frac{2}{B\,Y_0}\right] \quad (15)$$

Similarly, for one series reactive element

$$Z/Z_0 = 1 + jX/Z_0 \quad (16)$$

Is transformed to $Z/Z_0 = 1 - jX\,Z_0$ (17)

By a displacement of

$$? = \frac{\lambda}{2\pi} \tan^{-1} \left[\frac{2}{X/Z_0}\right] \quad (18)$$

A second equal reactive element spaced a distance ? from the first would result in minimum insertion loss.
For maximum attenuation, the second equal reactive element placed where the impedance of the first is transformed to

$$\left[\frac{1}{1-jX/Z_0}\right] \quad (19)$$

Which is ? $\frac{\lambda \tan^{-1} 2}{2\pi} \quad \frac{+/4}{x/z_0}$ (20)

Power loss due to reflection is given by

$$X = \log (1+ R/Z_0)^2 + (X/Z_0)^2 \quad (21)$$

One series reactive element results in

$$Z/Z_0 = 1+ j\,(X/Z_0) \quad (22)$$

$$X_1 = 10\log \frac{4 + (X/Z_0)^2}{4} \quad (23)$$

And $(X/Z_0)^2 = 4(10X_1/10 -1)$

$$\frac{Z}{Z_0} = \frac{1}{1-j\,(X Z_0)} + j\,(X/Z_0)$$

$$\text{or } \frac{Z}{Z_0} = 1 + j\,(X Z_0)\frac{(2+(X Z_0)^2)}{1+(XZ0)^2} \quad (24)$$

Then we obtain that

$$X^2 = 10\log \frac{\left[\frac{1}{1+(X/Z_0)^2}\right]^{+1}{}^2 + \left[\frac{X Z\,(2+X^2 Z^2_0)}{1+(X/Z_0)^2}\right]^2}{4.\frac{1}{1+(X/Z_0)^2}} \quad (25)$$

$$\text{Or } X_2 = 20\log 2 + \frac{(X/Z_0)^2}{2} \quad (26)$$

$$X_1 = X_2 - 2X_1$$

$$= 20\log\left[\frac{2+(X/Z_0)^2}{2}\right] - 20\log\left[\frac{4+(XZ_0)^2}{4}\right] \quad (27)$$

$$\text{Or } X_1 = 20\log\left[\frac{4+2(X/Z_0)^2}{4+(X/Z^0)^2}\right]$$

$$= 20\log (2 - 10^{-(x1/10)}) \quad (28)$$

For the maximum attenuation from two or more shunt

$$Y_2 = \frac{1}{1-j\,(B/Y_0)} + j\,(B/Y_0)$$

$$= 1 + j2B/Y_0 \quad (29)$$

$$Y_n = 1 + j_n\,(B/Y_0)$$

$$X = 10\log \frac{(1+G/G_0)^2 + (B/Y_0)^2}{4(G/Y_0)}$$

$$= 10\log (1+n^2 B^2/rY^2_0) \quad (30)$$

The calculation for the extra attenuation resulting from the third or higher additional identical optimum spaced elements is simplified by the fact that the addition of equal reactance or susceptance results in a total impedance or admittance which has repeatedly the same reflection coefficient angle and that the corresponding reciprocal of the complex conjugate of the impedance has another repeating reflection coefficient angle. Thus, the total impedance or admittance for one more element can be found by taking the reciprocal of the complex conjugate of the total impedance or admittance from the addition of the last element and then adding the new element. The extra attenuation for the second, third and fourth additional element as well as the limit for large number of elements can easily be evaluated from a plot. The total attenuation for N elements is given by

$$X_{t=nx_1} + \sum_{1=2}^{n} X_n \quad (31)$$

3.2 Single Pole thro Switch

To test the above design theory, two single diode switching circuits were constructed on polygide substrate which has a 1.0z sheet of copper bonded on one side and a 0.625cm thick aluminum plate bonded on the other side. The aluminum provides the necessary mechanical stabilization and also serves as a mounting structure for the connectors and a heat sink for the diodes. A three element bias filter was used for the bias signal. This was situated at the output side of the diode so that power should be reflected from the

port that this is connected to the diode module. The main function of the bias filter is to block the passage of the radio frequency signals into the bias line and at the same time allow the d.c signal from the bias port to reach the device. The d.c block used is a 100pF chip capacitor and two of these are located at the input and output parts respectively. The overall circuit is shown in fig

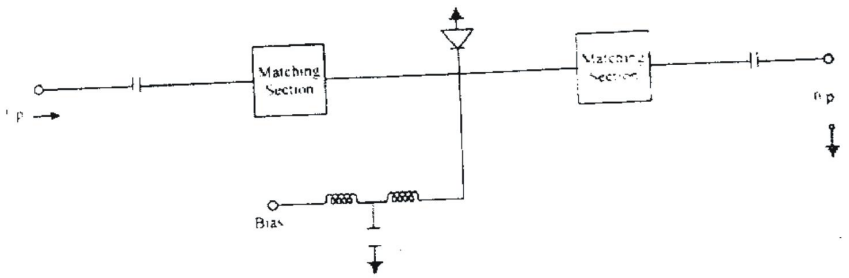

Fig 6: Single pole single pole switch

The matching sections of the circuit are 35 ohms quarterwave transforms designed to match the load to the characteristic impedance of the line. The diode was located at a length " from the input port such that $60^0 < 120^0$ throughout the operating band. The circuit responses were then measured over the frequency band 2-4GHz in steps of 200MHz. Fig. 7 shows the variations of the insertion loss of the diode with frequency when the diode is reverse biased. The response shows a minimum transmission coefficient S_{21} = 0.94 at 3.2GHz and a maximum reflection coefficient S_{11} = 0.11 for the zero bias condition. When the bias is increased to -30V, the minimum transmission coefficient increased to 0.96 which is equivalent to 0.36dB insertion loss.

Figure 8 shows the variations of the isolation when a forward bias is applied to it. With 50mA bias current, the minimum isolation obtained was S_{21} = 0.093 or 20.6dB. When the bias was reduced to 15mA, this reduced to S_{21} = 0.12 or 18.4dB. To obtain maximum isolation, the forward bias conductance should be as large as possible. This implies that the forward bias current should completely saturate the intrinsic region with charge, this producing the highest conductance level. To investigate the above phenomenon, various bias levels were used to bias the diode. Figure 9 shows the results obtained. As can be seen, the isolation increases proportionally as the current is increased from 0 – 10mA. However above 10mA, any increase in the bias current produces on a small increase in value of isolation.

Figure 10(a) shows a two or three diode circuit. The diodes were biased separately as shown in the figure. The length of the transmission line separately the diodes was made a quarter wavelength at 3GHz. The circuit was measured using bias current of 30mA and a

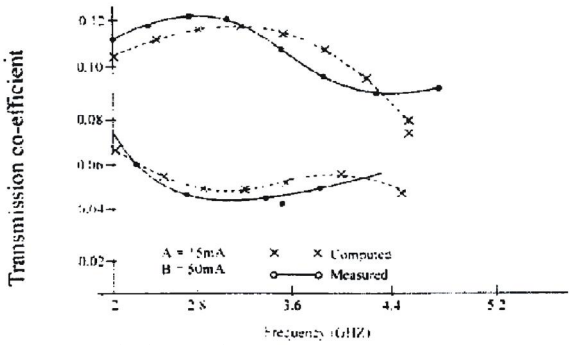

Fig. 7 variation of insertion loss with frequency

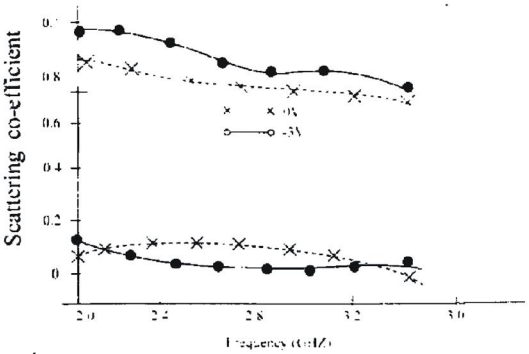

Fig. 8 Variation of isolation with frequency

Diode is show in fig. 10(b)

For the case of N = 2, the transmission coefficient has a minimum of S_{21} = 0.92 or 0.72dB compared to S_{11} = 0.07. An isolation of

44dB was obtained with 2 diodes over a 30 percent bandwidth compared to 53.9dB for 3 diodes

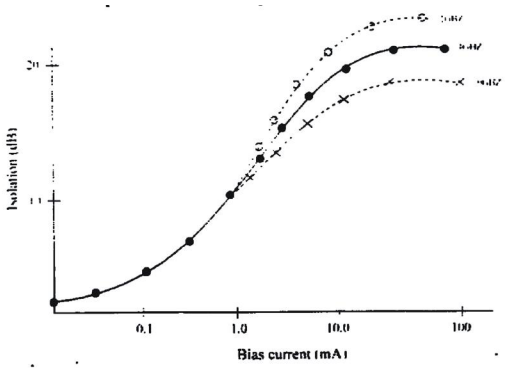

Fig. 9: Variation of isolation with bias current

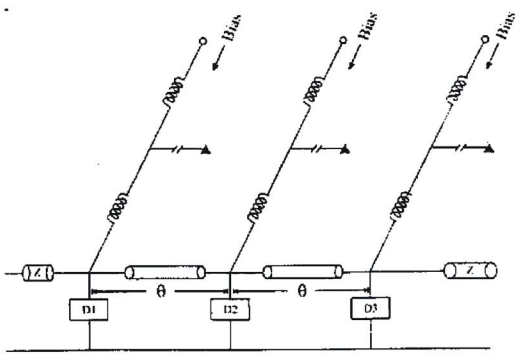

Fig. 10: Multiple diode switch

CONCLUSION

Transmission at microwave frequencies has been used and is still being applied in many systems today. The use of lumped elements has made it possible to use semiconductor device effectively at these wavelengths. The use of the p-i-n diode in single and multiple microstrip diode simulating elements has been used to obtain the base characteristic of transmission line parameters. It is expected that from the work done ultra band systems using multiple throw switches to cover frequency bands of several octares simultaneously will be possible. This design and production of single pole double throw switches are possible.

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